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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,378	03/29/2004	Yi-Hsun Wu	N1280-00120(TSMC2003-0919	2646

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EXAMINER	
BAUER, SCOTT ALLEN	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,378	WU ET AL.	
	Examiner	Art Unit	
	Scott Bauer	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-11, 13, 14, 16 & 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (US 6,521,952) in view of Lee et al. (US 6,066,879).

3. With regard to Claims 1-3, Ker et al., in Fig. 11a, teaches an input and output (I/O) circuit comprising: an output buffer (702) having an NMOS transistor coupled to a PMOS transistor; an ESD protection circuit (714) having a parasitic silicon controlled rectifier (SCR) integrated therein, and coupled to the output buffer; and a diode string (716) having a predetermined number of diodes coupled between a cathode of the SCR and ground, wherein a voltage drop across the diode string increases the SCR holding voltage (column 13 lines 41-46), thereby setting an ESD protection holding voltage for the ESD protection circuit and that the number of diodes in the diode string is determined by a positive supply voltage and the SCR holding voltage (column 13 lines 41-44).

Ker et al. does not teach that the diode string is coupled between a source node of the NMOS transistor and ground or that the NMOS transistor is realized by using two asymmetric NMOS transistors.

Lee et al., in Figures 3 & 4, teaches a combined NMOS and SCR ESD protection device wherein two DENMOS transistors (Q5 & Q6), which are asymmetric NMOS transistors, are used to realize an NMOS transistor and that an SCR is formed between the two DENMOS transistors (column 2 lines 57-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ker et al. with Lee et al., by replacing the discrete SCR and NMOS transistor taught by Ker et al., with the combined NMOS and SCR ESD protection device taught by Lee et al., for the purpose of reducing the footprint of the ESD device and to reduce the snap-back voltage of the device (column 3 lines 33 & 34). In the circuit taught by Ker et al. in view of Lee et al., the asymmetric NMOS transistors are in parallel with the SCR as see in Lee et al. Figure 4. The diode chain is coupled between the common node shared by the sources of the NMOS transistors and the cathode of the SCR and ground.

4. With regard to Claim 8, Ker et al. in view of Lee et al. discloses an input and output (I/O) circuit comprising: an output buffer having an NMOS transistor coupled to a PMOS transistor; an ESD protection circuit having a parasitic silicon controlled rectifier (SCR) integrated therein and coupled to the output buffer; and a diode string having four, or fewer diodes, coupled between a source node of the NMOS transistor and

ground, wherein a voltage drop across the diode string increases the SCR holding voltage, thereby setting an ESD protection holding voltage for the ESD protection circuit.

5. With regard to Claim 13, Ker et al. in view of Lee et al. discloses a layout for an output buffer having an NMOS transistor comprising: a N well region (Lee et al. Fig. 3 30) having a P+ region contained therein (36); and two asymmetrical NMOS transistors (Q5 & Q6) formed on two sides of the P+ region; wherein a portion of the P+ region in the N well region provides at least one resistor (R1) for a parasitic silicon controlled rectifier (SCR), and wherein a diode string (Ker et al., 716) having a predetermined number of diodes is coupled between a source node of the NMOS transistors and ground.

6. With regard to Claims 4 & 11 Ker et al. in view of Lee et al. discloses the circuit of Claim 1. Lee et al. further discloses that the NMOS transistor is realized by using a transistor layout for enhancing a turn-on speed of the ESD protection circuit. In paragraph 0018 of the specification, Applicant discloses that two parallel asymmetric NMOS transistors may be utilized to form the NMOS transistor in order to decrease the inherent capacitance, thereby increasing the circuit switching speed. Lee et al., in figure 4, teaches the use of two asymmetric transistors to form a transistor, which is a layout for enhancing a turn-on speed of the ESD protection circuit.

7. With regard to Claims 6, 7, 16 & 17, Ker et al. in view of Lee et al. discloses the circuit of Claim 1. Ker et al. further discloses that the diode string has two or fewer diodes. Ker et al. discloses that the diode chain comprises (D_1 to D_n) diodes (column 13 line 44), which can be two or less.

Further, Ker et al. in view of Lee et al. discloses the claimed invention except that the diode chain sets a positive supply voltage of about 2.5 V or less. It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the holding voltage of the SCR for different input voltages, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

8. With regard to Claims 9 & 14, Ker et al. in view of Lee et al. discloses the circuit of Claim 8 & 13. Ker et al. further discloses that the number of diodes in the diode string is determined by a positive supply voltage and the SCR holding voltage (column 13 lines 41-44).

9. With regard to Claim 10, Ker et al. in view of Lee et al. discloses the circuit of Claim 8. Lee et al. further discloses that the NMOS transistor is realized by using two asymmetric transistors (column 2 lines 57-67).

10. Claims 5, 12, 15, 18 & 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (US 6,521,952) in view of Lee et al. (US 6,066,879) and further in view of Ker et al. (US 5,473,169).

11. With regard to Claims 5, 12 & 15, Ker et al. (US 6,521,952) in view of Lee et al. discloses the circuit of Claim 1.

Ker et al. (US 6,521,952) in view of Lee et al. does not teach that the SCR has an increased beta-gain product of two transistors therein.

Ker et al. (US 5,473,169), teaches an ESD protection circuit wherein the spacing between wells that form the SCR should be optimized by shorter spacing to increase there beta gains (column 5 lines 36-49).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ker et al. (US 6,521,952) in view of Lee et al. with Ker et al. (US 5,473,169), by increasing the beta gains of the BJT's that make up the SCR taught by Ker et al. (US 6,521,952) in view of Lee et al., for the purpose of improving the latching performance of the SCR (Ker et al. (US 5,473,169) column 5 lines 38-39).

12. With regard to Claim 18, Ker et al. (US 6,521,952) in view of Lee et al. (US 6,066,879) teaches the circuit of Claim 13.

Ker et al. (US 6,521,952) in view of Lee et al. (US 6,066,879) does not teach that the circuit further comprises one or more guard rings to collect minority carriers.

Ker et al. (US 5,473,169), teaches the use of a guard ring around an ESD protection circuit (column 28–32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ker et al. (US 6,521,952) in view of Lee et al. (US 6,066,879) with Ker et al. (US 5,473,169), by surround the circuit of Claim 13 with a guard ring, for the purpose of preventing latch-up (Ker et al. (US 5,473,169), column 3 lines 28-32).

13. With regard to Claim 19, Ker et al. (US 6,521,952) in view of Lee et al. (US 6,066,879) teaches the layout of Claim 13.

Ker et al. (US 6,521,952) in view of Lee et al. does not teach that a center portion of the P+ region is connected to an input/output pad..

Ker et al. (US 5,473,169), in Figure 1, teaches an SCR circuit (20) wherein its anode is connected to an I/O pad.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ker et al. (US 6,521,952) in view of Lee et al. with Ker et al. (US 5,473,169), by connecting the anode (36) of the SCR taught by Ker et al. (US 6,521,952) in view of Lee et al. to an I/O pad, for the purpose of providing ESD protection to an I/O pad.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAB
02/09/2006

PHUONG T. VU
PRIMARY EXAMINER